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10/773,026	02/05/2004	Qi Xiang	039153-0649	6093

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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,026	XIANG ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Applicant's amendment to claim 15 has overcome the objection made in the previous Office Action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghyselen et al. (U.S. 2004/0053477) in view of Cabral, Jr. et al. (U.S. 2005/0059242), with Tong et al. (*Semiconductor Wafer Bonding*, Wiley-Interscience, 1998) used as a definition for claim 19.

Regarding claim 11, Ghyselen et al. teaches a method of making a structure, the method comprising providing a first semiconductor substrate including a base layer (**1** in Fig. 2b), a strained semiconductor layer (**3** in Fig. 2b), a semiconductor/germanium layer (**2** in Fig. 2b) and a first oxide layer (not pictured—paragraph 0080), wherein the semiconductor/germanium layer is above the strained semiconductor layer (Fig. 2b); attaching a second semiconductor substrate (**4** in Fig. 2c) including a second oxide layer (paragraph 0080) to the first oxide layer; and separating the base layer from the first substrate (Fig. 2d; paragraph 0085). The phrase "method of making an IC structure containing a plurality of transistors" has not been given patentable weight because it

appears in the claim preamble, and none of the process steps recited in claim 1 relate to this preamble. Furthermore, the structure formed by the method taught by Ghyselen et al. could be used to make an IC structure containing a plurality of transistors, since the method taught by Ghyselen et al. is identical to the method claimed in Applicant's claim 1.

Ghyselen et al. does not teach siliciding the semiconductor/germanium layer.

Cabral, Jr. et al. teaches siliciding a silicon germanium layer of a substrate in order to reduce the resistance of this layer for the purposes of making device contacts (paragraphs 0002 and 0011).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Ghyselen et al., and then silicide the SiGe layer, as taught by Cabral, Jr. et al, in order to reduce the resistance of this layer for the purpose of making device contacts.

Regarding claim 19, Ghyselen et al. and Cabral, Jr. et al. together teach the method of claim 11. Ghyselen et al. further teaches that the attaching step is a hydrogen bonding step (paragraph 0077 teaches bringing the receiving substrate into intimate contact with the strained silicon film—or oxide layer, as taught by paragraph 0080—and carrying out bonding, which is hydrogen bonding. See pp. 80-87 of Tong et al., *Semiconductor Wafer Bonding*, 1998, referenced by Ghyselen et al. in paragraph 0077).

Regarding claim 20, Ghyselen et al. teaches a method of manufacturing an integrated circuit, the integrated circuit comprising a first wafer (Fig. 2b) and a second

wafer (layer **4** in Fig. 2c), the first wafer including a silicon germanium layer (**2** in Fig. 2b), a strained silicon layer (**3** in Fig. 2b), and a first insulating layer (paragraph 0080), the second wafer including a substrate (**4** in Fig. 2c) and a second insulating layer (paragraph 0080), the second insulating layer being attached to the first insulating layer (paragraph 0080), the method comprising the steps of (paragraphs 0071-0085) providing the first wafer including the silicon germanium layer, the strained silicon layer, and the first insulating layer (Fig. 2b; paragraph 0080); attaching the second wafer to the first wafer (Fig. 2c); and separating base layer from the first wafer (Fig. 2d; paragraph 0085).

Ghyselen et al. does not teach siliciding the semiconductor/germanium layer.

Cabral, Jr. et al. teaches siliciding a silicon germanium layer of a substrate in order to reduce the resistance of this layer for the purposes of making device contacts (paragraphs 0002 and 0011).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Ghyselen et al., and then silicide the SiGe layer, as taught by Cabral, Jr. et al, in order to reduce the resistance of this layer for the purpose of making device contacts.

Regarding claims 21 and 22, Ghyselen et al. and Cabral, Jr. et al. together teach the method of claim 20. Ghyselen et al. further teaches that the substrate is a bulk silicon substrate, which is a semiconductor material (paragraph 0071).

Regarding claim 23, Ghyselen et al. and Cabral, Jr. et al. together teach the method of claim 22. Ghyselen et al. further teaches that the silicon germanium layer includes a hydrogen-breaking interface (paragraph 0094).

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghyselen et al. (U.S. 2004/0053477) in view of Cabral, Jr. et al. (U.S. 2005/0059242), as applied to claim 20 above, and further in view of Ge et al. (U.S. 6,900,502).

Regarding claims 24 and 25, Ghyselen et al. and Cabral, Jr. et al. together teach the method of claim 20 (note 35 U.S.C. 103(a) rejection above), but do not teach that a channel region or a source and drain region are disposed in the strained silicon layer.

Ge et al. teaches forming a channel region (**30** in Fig. 1) and source and drain regions (**24** and **26** in Fig. 1) in a strained silicon layer (**18** in Fig. 1; column 3, lines 28-31 and 53-57) because strained silicon has higher carrier mobility than relaxed silicon (Ge et al., column 1, lines 24-61; Ghyselen et al., paragraph 0034).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the strained silicon layer taught by Ghyselen et al. and Cabral, Jr. together as a channel and source/drain layer, as taught by Ge et al., since strained silicon layers are known to have increased carrier mobility, as taught by Ge et al. and Ghyselen et al., which results in improved device performance.

Claims 12-18, and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghyselen et al. (U.S. 2004/0053477) in view of Cabral, Jr. et al. (U.S. 2005/0059242) and Gardner (U.S. 5,801,075).

Regarding claim 28, Ghyselen et al. teaches a method of fabricating a multilayer structure, the method comprising providing a first substrate including a silicon/germanium layer (**5** in Fig. 2d; paragraph 0085), a strained semiconductor layer (**3** in Fig. 2b), and a first oxide layer (not pictured—paragraph 0080); and attaching a second substrate (**4** in Fig. 2c) including a second oxide layer (paragraph 0080). Ghyselen et al. does not teach providing a silicide layer above the SiGe layer. Ghyselen et al. also does not teach providing an aperture within the semiconductor/germanium layer and providing a gate dielectric and gate conductor within the aperture.

Cabral, Jr. et al. teaches siliciding a silicon germanium layer of a substrate in order to reduce the resistance of this layer for the purposes of making device contacts (paragraphs 0002 and 0011).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method taught by Ghyselen et al., and then silicide the SiGe layer, as taught by Cabral, Jr. et al, in order to reduce the resistance of this layer for the purpose of making device contacts.

Gardner et al. teaches a method of forming a trench transistor in a multilayered substrate comprising the steps of providing an aperture in the top substrate layer (N+ layer in Fig. 1D; column 5, lines 48-63); and providing a gate dielectric (**130** in Fig. 1J) and gate conductor (**138** in Fig. 1J) within the aperture. This method produces a transistor with a channel length that is smaller than the minimum resolution available with photolithography (column 4, lines 37-41), which allows more devices to be manufactured per chip (column 1, lines 40-43).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method of forming an IGFET taught by Gardner et al. with the method to form a substrate including a semiconductor/germanium layer and strained silicon layer taught by Ghyselen et al. and Cabral, Jr. et al. together to result in a method of fabricating a multilayer structure containing a plurality of transistors including strained regions, the multilayer structure comprising a semiconductor/ germanium layer and a strained semiconductor layer, a gate dielectric, and a gate conductor, the semiconductor/germanium layer having an aperture, the gate dielectric above the strained semiconductor layer and within the aperture, the gate conductor being disposed within the aperture. The phrase "including a source and drain provided below the semiconductor/germanium layer" has not been given patentable weight because it appears in the claim preamble, and none of the method steps recited in claim 28 relate to this portion of the preamble.

The motivation for doing so at the time of the invention would have been to use the substrate taught by Ghyselen et al. and Cabral, Jr. et al. together to fabricate a transistor with a channel length that is smaller than the minimum resolution available with photolithography, which allows more devices to be manufactured per chip, as expressly taught by Gardner et al.

Regarding claim 12, Ghyselen et al., Cabral, Jr. et al., and Gardner et al. together teach the method of claim 28. Ghyselen et al. further teaches that the semiconductor-germanium layer is above the strained semiconductor layer (Fig. 2b).

Regarding claims 13-17, Ghyselen et al. Cabral, Jr. et al., and Gardner et al. together teach the method of claim 12. Gardner et al. further teaches a method of forming a trench transistor in a multilayered substrate comprising the steps of providing an aperture in the top substrate layer (N+ layer in Fig. 1D; column 5, lines 48-63), doping the underlying layer through the aperture (Fig. 1E; column 5, line 64 – column 6, line 1), wherein the doping step forms source and drain extensions (**352A**, **352B** in Fig. 3E), providing a gate conductor in the aperture (**136** in Fig. 1J; column 7, lines 19-24), and separating the gate conductor from the top substrate layer (spacers **126A** and oxide **132A** in Fig. 1J (column 7, lines 7-18). This method produces a transistor with a channel length that is smaller than the minimum resolution available with photolithography (column 4, lines 37-41), which allows more devices to be manufactured per chip (column 1, lines 40-43).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method to fabricate an IGFET taught by Gardner et al. with the substrate taught by Ghyselen et al. and Cabral, Jr. et al. together, wherein the top layer is the silicon germanium layer and the underlying layer is the strained silicon layer, to result in the invention as specified in claims 13 (providing an aperture in the silicon/germanium layer), 14 (doping the strained silicon layer through the aperture), 16 (providing a gate conductor in the aperture), and 17 (separating the gate conductor from the silicon/germanium layer with a spacer material). The motivation for doing so at the time of the invention would have been to fabricate a transistor with a channel length that

is smaller than the minimum resolution available with photolithography, which allows more devices to be manufactured per chip, as expressly taught by Gardner et al.

Regarding claims 18 and 30, Ghyselen et al., Cabral, Jr. et al., and Gardner et al. together teach the method of claims 12 and 28. Gardner et al. further teaches etching the top layer—in this combination of references the top layer is the SiGe layer—and later forming a contact window in the oxide layer above the source and drain regions formed in this layer (column 5, lines 48-63; column 11, lines 48-53). Cabral, Jr. et al. additionally teaches siliciding a SiGe layer to lower its resistance in order to form contacts for a device.

Therefor, at the time of the invention, it would have been obvious to use the method taught by Ghyselen et al., Cabral, Jr. et al., and Gardner et al., and further etch the semiconductor/germanium layer, as taught by the combination of Ghyselen et al, and Gardner et al., and then silicide the SiGe layer, as taught by the combination of Gardner et al. and Cabral, Jr.

The motivation for doing so at the time of the invention would have been to fabricate a transistor with a channel length that is smaller than the minimum resolution available with photolithography, which allows more devices to be manufactured per chip, as expressly taught by Gardner et al., and additionally provide low-resistance contacts to the device, as taught by Cabral, Jr.

Regarding claim 29, Ghyselen et al., Cabral, Jr. et al. and Gardner et al. together teach the method of claim 28. Gardner et al. further teaches providing a spacer in the aperture separating the top substrate layer and the gate conductor (**126A**, **126B**, **132A**,

and **132B** in Fig. 1J). As combined with Ghyselen et al. and Cabral, Jr. et al. in claim 28, this top layer is the semiconductor/germanium layer.

Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghyselen et al. (U.S. 2004/0053477) in view of Cabral, Jr. et al. (U.S. 2005/0059242) and Ge et al. (U.S. 6,900,502) as applied to claim 25 above, and further in view of Gardner et al. (U.S. 5,801,075).

Regarding claims 26 and 27, Ghyselen et al., Cabral, Jr. et al., and Ge et al. together teach the method of claim 25 (note 35 U.S.C. 103(a) rejection above), but do not teach that an aperture is formed in the silicon germanium layer to expose the strained silicon layer, or that a gate structure is provided in the aperture.

Gardner et al. teaches a method of forming a trench transistor in a multilayered substrate comprising the steps of providing an aperture in the top substrate layer (N+ layer in Fig. 1D; column 5, lines 48-63), and providing a gate structure in the aperture (conductor **136** and oxide **130** in Fig. 1J; column 7, lines 19-24). This method produces a transistor with a channel length that is smaller than the minimum resolution available with photolithography (column 4, lines 37-41), which allows more devices to be manufactured per chip (column 1, lines 40-43).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Ghyselen et al., Ge et al., and Gardner et al., to form an integrated circuit according to the method taught by Ghyselen et al. and Ge et al. together, and also taught by claim 25, and further form an aperture in the top layer (silicon germanium) to expose the underlying (strained silicon) layer, and

then form a gate structure in the aperture, as taught by Gardner et al. The motivation for doing so at the time of the invention would have been to fabricate a transistor with a channel length that is smaller than the minimum resolution available with photolithography, which allows more devices to be manufactured per chip, as expressly taught by Gardner et al.

Response to Arguments

Applicant's arguments with respect to claims 11-30 have been considered but are moot in view of the new ground(s) of rejection.

This Office action is made non-final to allow Applicant to respond to the new grounds of rejections.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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